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IN THE SPECIFICATION

Please amend the spelling in paragraph 2 as follows:

[0002] Microprocessors often use instruction pipelining to increase instruction throughput. An instruction pipeline processes several instructions through different stages of instruction execution concurrently, using an assembly line-type approach. The pipeline stages are often controlled by predicate registers. One predicate register may be assigned to each stage in the pipeline. All instructions for that stage may then share the same predicate register. Thus, this enables determination of whether the instructions for the stage are executed or not. In other applications, such as ~~Itanium application~~ Itanium applications, each instruction (referred to as "syllable") has its own "qualifying predicate" that determines whether it executes or not.

Please amend the spelling in paragraph 32 as follows:

[0032] In an alternative embodiment, when an all-predicates writing instruction is encountered, the processor may determine if there are any pending writes (*e.g.*, busy bits set) in the currently selected predicate register file. This may be done by OR-ing the busy bits of the selected

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predicate register file's scoreboard. If no busy bits are set, then no new predicate register file ~~need~~ needs to be allocated since no WAW dependencies exist. This may conserve the use of the predicate register files at the cost of performing the WAW check. If any of the busy bits are set, a new predicate register file may be allocated in the same manner as in the illustrated embodiment of FIG. 4. Hence, the processor does not have to stall for any WAW dependencies.